



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,074	09/23/2003	Judson E. Veazey	200205496-1	2708

22879 7590 04/15/2009

HEWLETT PACKARD COMPANY  
P O BOX 272400, 3404 E. HARMONY ROAD  
INTELLECTUAL PROPERTY ADMINISTRATION  
FORT COLLINS, CO 80527-2400

EXAMINER
----------

LUU, CUONG V

ART UNIT	PAPER NUMBER
----------	--------------

2128

NOTIFICATION DATE	DELIVERY MODE
-------------------	---------------

04/15/2009

ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

JERRY.SHORMA@HP.COM  
ipa.mail@hp.com  
jessica.l.fusek@hp.com

<b>Office Action Summary</b>	<b>Application No.</b> 10/669,074	<b>Applicant(s)</b> VEAZEY ET AL.	
	<b>Examiner</b> CUONG V. LUU	<b>Art Unit</b> 2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 19 December 2008.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 26-41 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 26-41 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 June 2008 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

### **DETAILED ACTION**

Claims 26-41 are pending. Claims 1-25 have been canceled. Claims 26-41 have been added. Claims 26-41 have been rejected.

### ***Response to Amendment***

1. In the reply filed on 12/19/2008, the Applicant indicates in the Remarks that amendment to the drawing has been amended; however, the Examiner cannot find the amended figure in the response by the Applicant.
2. The amendments to renumber the claims filed on 12/19/2008 has been considered and accepted.
3. The amendments to claim 29 to correct its dependence to claim 26 instead of canceled claim 3 filed on 12/19/2008 has been considered and accepted.

### ***Response to Arguments***

4. The objections to claims 27-39 have been withdrawn in light of amendments to them.
5. Applicant's arguments regarding claim 26, see pages 5-6, filed 12/19/2009 have been fully considered but they are not persuasive. The Applicant argues that Warn's teaching relates to the response time or the time that the transaction take to occur within the system while claim 26 recites the rate of input/output transactions in said input/output section is exponentially related to the amount of internal memory. The Examiner respectfully disagrees. In this document Warn teaches response time of an I/O transaction due to I/O access as described on page 81 col. 2 paragraph 2 and

Art Unit: 2128

Fig. 4 and on page 75 col. 1 and 2 section The Model. In these paragraphs, Warn shows relationship between amount of memory and response time by an exponential function. This teaching translates to I/O transaction rate is exponentially related to amount of internal memory. The Applicant also argues that a system may have a very long response time, but be able to have many input/output transactions occurring because it is able to operate with the long response time. For example, parallel transactions or cued transaction rates are not affected by the response time after equilibrium is achieved. Thus, the response time and the transaction rate are not necessarily related as suggested by the office action. The Examiner has to interpret a claim as broadly as possible, so as long as Warn's teaching read or suggest the limitation under broad's interpretation, the claim is rejected. Claim 26, therefore, remains rejected.

6. Claim 34 is argued allowable for the same ground as those of claim 26. For the same reasons discussed in item 4, claim 34 remains rejected.
7. Claims 27-33 and 35-41 are argued allowable for depending on claims 26 and 34, respectively. Since claims 26 and 34 remain rejected, claims 27-33 and 35-41 remain rejected.

### ***Drawings***

8. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled

Art Unit: 2128

"Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

**Claims 26-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Warn et al. (A Straightforward Model for Computer Performance Prediction, Computing Surveys Vol. 7, No. 2 June 1975).**

Art Unit: 2128

9. As per claim 26, Warn teaches a computer system comprising:

internal memory (p. 80, section Hardware Configuration Changes, paragraph 1);  
and

an input/output section (p. 75 col. 1, section The Model, paragraph 1);  
but does not teach the rate of input/output transactions in said input/output section is exponentially related to the amount of internal memory.

However, Warn teaches the input/output transaction response time is exponentially related to the internal memory (p. 75 col. 1 and 2 section The Model and p. 81 col. 2 paragraph 2 and Fig. 4). Transaction rate is the inversely proportional to transaction's response time, so it would have been obvious to one of ordinary skill in the art to be able to relate the transaction rate to the internal memory exponentially based on Warn's teachings. By relating the transaction rate to the internal memory, it would have facilitated the calculation of number of terminal devices can be connected to I/O section (p. 81 col. 1 paragraph 2).

10. As per claim 27, Warn teaches CPU time used for I/O transactions reaches an asymptotic limit for said rate of input/output transactions (p. 81 Fig. 4). This teaching implies the relation between the rate of input/output transactions and the amount of memory includes an asymptotic limit for said rate of input/output transactions.

11. As per claim 28, Warn, as discussed in claim 27, implies asymptotic limit for said rate of input/output transactions, and together with the exponential function relationship between the rate of input/output transactions and the amount of memory, it is obvious that a maximum rate of said input/output transactions is included.

Art Unit: 2128

12. As per claim 29, Warn suggests the relation between the rate of input/output

transactions and the amount of memory includes:

a maximum rate of input/output transactions;

an asymptotic limit for said rate of input/output transactions; and

an exponential decay from said maximum transaction rate to said asymptotic limit as a function of an amount of said internal memory.

On page 78 col. 1 equations 2-3 & 2-4 and page 81 Fig. 4. On page 81 Fig. 4, Warn teaches the exponential relationship between the transaction rate and sizes of memory. From the graph, one of ordinary skill in the art would have been able to provide a function of form  $a + e^{(c+bx)}$  to express it. Then from equations 2-3 & 2-4, throughput/transaction rate can be derived also in a form  $d + e^{(f+gx)}$ . These d, e, and g parameters are corresponding to a maximum rate of input/output transactions, an asymptotic limit for said rate of input/output transactions, and an exponential decay from said maximum transaction rate to said asymptotic limit as a function of an amount of said internal memory.

13. As per claim 30, these limitations have already been discussed in claim 29. They are, therefore, rejected for the same reasons.

14. As per claim 31, Warn teaches at least one storage device to support said input/output transaction rate (p. 75 Fig. 1).

15. As per claim 32, Warn teaches at least one bus for communication between said storage device and said computer system to support said input/output transaction rate (p. 75 Fig. 1).

16. As per claim 33, it is common knowledge that an external storage device communicates with a computer via an interface card. This claim is, therefore, rejected.
17. As per claim 34, these limitations have already been discussed in claim 26. They are, therefore, rejected for the same reasons.
18. As per claim 35, these limitations have already been discussed in claim 27. They are, therefore, rejected for the same reasons.
19. As per claim 36, these limitations have already been discussed in claim 28. They are, therefore, rejected for the same reasons.
20. As per claim 37, these limitations have already been discussed in claim 29. They are, therefore, rejected for the same reasons.
21. As per claim 38, these limitations have already been discussed in claim 30. They are, therefore, rejected for the same reasons.
22. As per claim 39, these limitations have already been discussed in claim 31. They are, therefore, rejected for the same reasons.
23. As per claim 40, these limitations have already been discussed in claim 32. They are, therefore, rejected for the same reasons.



24. As per claim 41, these limitations have already been discussed in claim 33. They are, therefore, rejected for the same reasons.

### **Conclusion**

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cuong V. Luu whose telephone number is 571-272-8572. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah, can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. An inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published

Art Unit: 2128

applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**/Cuong V Luu/**

**Examiner, Art Unit 2128**

**/Hugh Jones/**

**Primary Examiner, Art Unit 2128**